REMARKS

Claims 25-30 are novel over Kinsman (6,172,419).

Regarding Claim 25, the Examiner states:

> Kinsman discloses a semiconductor package with **(25)** a substrate (102) having a first surface, an opposite second surface, and central throughhole between the first and second surfaces;
> a plurality of electrically conductive circuit patterns (106, 112) on each of the first and second surfaces of the substrate (102), **wherein the circuit patterns (106, 112) of each of the first and second surfaces of the substrate (106, 112) include a plurality of lands, the circuit patterns of the first surface also including a plurality of bond fingers**, ... (Office Action, page 2, emphasis added.)

The Examiner's statement is respectfully traversed. The Examiner has failed to callout where Kinsman teaches or suggests that **the circuit patterns on the first surface** of the substrate include **a plurality of lands** in addition to the plurality of bond fingers.

Specifically, Kinsman teaches:

> BGA package 100 comprises a substrate 102 having top **conductive traces 104 formed on an upper surface of substrate 102**. ... Bottom conductive traces 106 are formed on a lower surface of substrate 102 and are electrically connected to top conductive traces 104 through vias or plated through-holes 108. ... **Top conductive traces 104 terminate with bond posts or pads 110. Bottom conductive traces 106 terminate with ball or terminal pads 112. ...**
> Conductive solder balls 128 are each attached to a ball pad 112. (Col. 4, line 28 to col. 5, line 13, emphasis added.)

For at least the above reasons, the Examiner has failed to callout where Kinsman teaches or suggests:

> A stackable semiconductor package comprising:
> **a substrate having a first surface**, an opposite second surface, and central throughhole between the first and second surfaces;

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> a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, **wherein the circuit patterns of each of the first** and second **surfaces** of the **substrate include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers**, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface;
>
> a semiconductor chip in said throughhole and electrically connected to the bond fingers, **wherein the semiconductor chip has a first surface with bond pads thereon,** and an opposite second surface, **the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate**, and the second surface of the semiconductor chip is flush with the second surface of the substrate; and
>
> a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant,

as recited in Claim 25, emphasis added. Accordingly, Claim 25 is allowable over Kinsman. Claims 26-30, which depend from Claim 25, are allowable for at least the same reasons as Claim 25.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Claims 31-33 are novel over Akram et al. (6,313,522).

Regarding Claim 35, the Examiner states:

> Akram discloses a stack of semiconductor packages with
>
> **(31)** a first semiconductor package comprising: (a) a substrate (18) having a first surface, an opposite second surface, and central through hole between the first and second surfaces; ... a semiconductor chip (24B) in said through hole and electrically connected to the bond fingers (27), ... (d) **a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers**, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant ... (Office Action, pages 4-5, emphasis added.)

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The Examiner's statement that Akrams et al. teaches "**a hardened encapsulant** within said through hole and covering the semiconductor chip and the bond fingers" is respectfully traversed. Specifically, the Examiner has failed to callout where such "a hardened encapsulant" is illustrated in FIGS. 2-6 or discussed in the corresponding description. Should the Examiner disagree, Applicants respectfully request that the Examiner cite where in Akrams et al. the "a hardened encapsulant" is discussed in reference to FIGS. 2-6 and the reference number or other structure corresponding to "a hardened encapsulant" in FIGS. 2-6.

For at least the above reasons, the Examiner has failed to callout where Akrams et al. teaches or suggests:

> A stack of semiconductor packages comprising:
> a first semiconductor package comprising: (a) a substrate having a first surface, an opposite second surface, and central throughhole between the first and second surfaces; (b) a plurality of electrically conductive circuit patterns on each of the first and second surfaces of the substrate, wherein the circuit patterns of each of the first and second surfaces of the substrate include a plurality of lands, the circuit patterns of the first surface also include a plurality of bond fingers, and at least some of the circuit patterns of the first surface are electrically connected through the substrate to some of the circuit patterns of the second surface that include respective ones of the lands; (c) a semiconductor chip in said throughhole and electrically connected to the bond fingers, wherein the semiconductor chip has a first surface with bond pads thereon, and an opposite second surface, the first surface of the semiconductor chip faces in a same direction as the first surface of the substrate, and the second surface of the semiconductor chip is flush with the second surface of the substrate; (d) **a hardened encapsulant within said through hole and covering the semiconductor chip and the bond fingers, wherein the lands of each of the first and second surfaces are outward of a perimeter of the encapsulant**; and (e) a plurality of electrically conductive balls, wherein each of the conductive balls is fused to a respective one of the lands of the first surface of the substrate; and

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> a second semiconductor package comprising a plurality of second electrically conductive balls, wherein the second semiconductor package is in a stack with the first semiconductor package, and the second electrically conductive balls of the second package each superimpose and are electrically connected to a respective one of the lands of the second surface of the substrate of the first semiconductor package,

as recited in Claim 31, emphasis added. Accordingly, Claim 31 is allowable over Akrams et al. Claims 32, 33, which depend from Claim 31, are allowable for at least the same reasons as Claim 31.

For the above reasons, Applicants respectfully request reconsideration and withdrawal of this rejection.

Conclusion

Claims 25-33 are pending in the application. For the foregoing reasons, Applicants respectfully request allowance of all pending claims. If the Examiner has any questions relating to the above, the Examiner is respectfully requested to telephone the undersigned Attorney for Applicant(s).

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on January 5, 2006.

Attorney for Applicant(s) — January 5, 2006 Date of Signature

Respectfully submitted,

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